REMARKS

In the Office Action mailed December 24, 2003, claim 32 was objected to and claims 28, 30, 31, 33, 34, 36–38, 41, 42, 44, 45, 47–51, 53–55, 57–61, 63 and 64 were rejected under 35 U.S.C. § 102(b) over U.S. Pat. No. 6,008,120 to *Lee*. Finally, claims 29, 52 and 62 were rejected under 35 U.S.C. § 103(a) over *Lee* in view of U.S. Pat. No. 5,494,854 to *Jain*.

Claim 32 is amended to replace "depositing silicon dioxide" with "a plasma enhanced chemical vapor deposition method." Support for the amendment can be found on page 4, lines 17–19 of the specification. No new matter is added by the amendment, and claims 28–64 are pending in the application. Reconsideration and withdrawal of the objections and rejections is respectfully requested in view of the amendment and the following remarks.

A. The Objection to Claim 32 is Addressed

Claim 32 was objected to as being repetitive in light of claim 31. The amendment makes the objection moot by replacing "depositing silicon dioxide" with "a plasma enhanced chemical vapor deposition method." Accordingly, withdrawal of the objection is respectfully requested.

B. The Rejection of the Claims under § 102 & 103 over *Lee* is Addressed

Claims 28, 30, 31, 33, 34, 36–38, 41, 42, 44, 45, 47–51, 53–55, 57–61, 63 and 64 were rejected under 35 U.S.C. § 102(b) over *Lee*. In addition, claims 29, 52 and 62 were rejected under 35 U.S.C. § 103(a) over *Lee* in view of *Jain*. These rejections are traversed on the ground that *Lee* does not qualify as prior art against the present application.

In the first preliminary amendment filed with the application November 20, 2001, the specification was amended to claim priority to U.S. Patent Application Serial No. 09/563,030 filed May 1, 2000, which was a continuation of US. Patent Application Serial No. 09/132,876 filed August 11, 1998, now U.S. Patent No. 6,077,784, which claimed priority from Taiwan Application No. 87110514, filed June 30, 1998. A certified copy of the Taiwanese priority application was filed in U.S. Patent Application Serial No. 09/132,876.

Lee was filed December 1, 1998 and claimed priority to parent application 09/120,630 filed July 22, 1998. Thus, even the parent filing date is after the June 30, 1998 filing date of the Taiwanese priority application. An English translation of the Taiwanese priority application, and a statement that the translation is accurate are enclosed herewith.

All the requisite papers have been supplied that are needed to show that the Taiwanese priority application overcomes the earliest possible filing date for *Lee*. Accordingly, withdrawal of the rejections of claims 28, 30, 31, 33, 34, 36–38, 41, 42, 44, 45, 47–51, 53–55, 57–61, 63 and 64 under § 102(b) over *Lee*, and claims 29, 52 and 62 under § 103(a) over *Lee* in view of *Jain*, is respectfully requested.

C. Conclusion

In view of all of the above, claims 28–64 are believed to be allowable and the case in condition for allowance, which action is respectfully requested. Should the Examiner be of the opinion that a telephone conference would expedite the prosecution of this case, the Examiner is requested to contact the attorney at the telephone number listed below.

No fees are believed to be required with this Response, and should any be required, please charge Deposit Account 50-1123. Should any extension of time be required, please consider this a petition therefore and charge the required fee to Deposit Account 50-1123.

Respectfully submitted,

January 21, 2004

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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	:	Wu et al.
Application No.	:	09/563,030
Filed	:	May 1, 2000
Title	:	CHEMICAL-MECHANICAL POLISHING METHOD
Grp./Div.	:	2825
Examiner	:	Victor V. Yevsikov
Docket No.	:	

STATEMENT BY TRANSLATOR UNDER 37 C.F.R. § 1.55

Assistant Commissioner for Patents Post Office Box 7068
Washington, D.C. 20231

Commissioner:

I hereby declare that I translated Taiwan Patent Application No. 87110514 to English, and a true copy and correct copy of the English-language translation is attached hereto.

I hereby, confirm that the English translation enclosed herewith is an accurate translation of Taiwan Patent Application No. 87110514 which was filed June 30, 1998.

I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Date Jan. 15, 2004

By _____
Jeff C. Cho

INTELLECTUAL PROPERTY OFFICE
MINISTRY OF ECONOMIC AFFAIRS
REPUBLIC OF CHINA

This is to certify that annexed is a true copy from the records of this Office of the application as originally filed which is identified hereunder:

Application Date: June 30, 1998

Application No. : 87110514

Applicant(s) : United Microelectronics Corp.

Director General

Ming-Pang CHEN

Issue Date :
Serial No :

Filing Date
Filing No.
Type

(The above column should be filled out by the IPO)

Patent / Utility Model Specification

1. Title of Patent / Utility Model	Chinese	CHEMICAL-MECHANICAL POLISHING METHOD
	English	
2. Inventor	Name	1. Kun-Lin Wu 2. Meng-Jin Tsai
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	Name of the Representative	Robert H.C. Tsao

CHEMICAL-MECHANICAL POLISHING METHOD

ABSTRACT OF THE DISCLOSURE

A chemical-mechanical polishing process for forming a metallic interconnect includes the steps of providing a semiconductor substrate having a first metallic line thereon, and then forming a dielectric layer over the substrate and the first metallic line. Next, a chemical-mechanical polishing method is used to polish the surface of the dielectric layer. Thereafter, a thin cap layer is formed over the polished dielectric layer. The thin cap layer having a thickness of between 1000-3000Å can be, for example, a silicon dioxide layer, a phosphosilicate glass layer or a silicon-rich oxide layer. The method of forming the cap layer includes depositing silicon oxide using a chemical vapor deposition method with silicane (SiH_4) or tetra-ethyl-ortho-silicate (TEOS) as the main reactive agent. Alternatively, the cap layer can be formed by depositing silicon nitride using a chemical vapor deposition method with silicane or silicon dichlorohydride (SiH_2Cl_2) as the main reactive agent. Finally, a via opening is formed through the dielectric layer and the cap layer, and a second metallic line that couples electrically with the first metallic line through the via opening is formed.

BACKGROUND OF THE INVENTION

Field of Invention

The present invention relates to a method of forming a metallic interconnect. More particularly, the present invention relates to a method of planarizing an inter-layer dielectric (ILD) layer or inter-metal dielectric (IMD) layer using a chemical-mechanical polishing (CMP) method.

Description of Related Art

In the fabrication of semiconductors such as very large scale integrated (VLSI) or ultra-large scale integrated (ULSI) circuits, usually two or more metallic layers are employed to interconnect semiconductor devices in different areas of a silicon chip. In general, inter-layer dielectric (ILD) or inter-metal dielectric (IMD) is used as an isolating material between metal lines in different layers. Therefore, as the design rules for forming semiconductor devices becomes highly restrictive due to miniaturization, the quality of the ILD or the IMD layer, such as its degree of surface planarity, is of growing importance.

In general, a high degree of surface planarity is an important factor in forming high-density devices using a photolithographic operation. Only a highly planar surface is capable of avoiding undesirable diffraction due to height difference during light exposure, so as to achieve a highly accurate pattern transfer. Planarization techniques can be categorized into two major groups, namely, a spin-on-glass (SOG) method and a chemical-mechanical polishing (CMP) method. However, when fabrication of semiconductors reaches the sub-half-micron stage, the spin-on-glass method is incapable of providing the degree of planarity necessary for high-quality production. Hence, the chemical-mechanical polishing method has become one of the principle means of global planarization in VLSI or ULSI production.

Figs. 1A through 1D are cross-sectional views showing the progression of manufacturing steps in producing a metallic interconnect that uses chemical-mechanical polishing according to a

conventional method. First, as shown in Fig. 1A, a semiconductor substrate 10 having an inter-layer dielectric (ILD) layer 12 thereon is provided. Then, a conductive line layer 14, for example, an aluminum layer or a polysilicon layer is formed over the ILD layer 12. Thereafter, an insulating layer 16 is formed by deposition over the ILD layer 12 and the conductive line layer 14. Preferably, the insulating layer 16 is formed using a high-density plasma chemical vapor deposition (HDPCVD) method. Due to the presence of the conductive lines 14 underneath, the insulating layer 16 has a pyramid-like cross-sectional profile 18 near its upper surface. In the subsequent step, an inter-metal dielectric (IMD) layer 19 is formed over the insulating layer 16.

Next, as shown in Fig. 1B, a chemical-mechanical polishing (CMP) operation is carried out to polish the IMD layer 19 so that a planar upper surface is obtained. Because a CMP method can easily lead to the over-polishing of the surface of the IMD layer 19 or the scratching of surface by polishing particles, micro-scratches will appear on the surface of the IMD layer 19. These micro-scratches vary in size and depth, and two such scratches 20a and 20b are shown in Fig. 1B.

Next, as shown in Fig. 1C, conventional photolithographic and etching operations are carried out to pattern the insulating layer 16. Consequently, an opening 22 through the insulating layer 16 and the IMD layer 19 is formed. The opening 22 exposes one of the conductive line layers 14 and subsequently will serve as a via.

Next, as shown in Fig. 1D, a metallic layer 26 is formed over the IMD layer 19 and inside the opening 22. Thereafter, photolithographic and etching operations are again carried out to pattern the metallic layer 26, thereby forming second metallic lines 26. Due to the presence of scratches (20a and 20b) on the surface of the IMD layer 19, metal will also be deposited into the scratches forming undesirable metallic scratch lines 24a and 24b.

The metallic scratch lines 24a and 24b can lead to a number of defects. Fig. 2 is a top view of a conventional metallic interconnect structure. In Fig. 2, first conductive lines 30, for example, an aluminum layer or a polysilicon layer, are formed over a semiconductor substrate (not shown in the

figure). In addition, second conductive lines 32 are formed above the first conductive lines 30. Through a via opening 33, the first conductive line 30 is connected to the second conductive line 32. If the surface for forming the first conductive line 30 is over-polished and scratches are formed, metallic scratch lines such as the one labeled 34 in Fig. 2 will form. The metallic scratch line can form a bridge linking up neighboring second conductive lines, thereby causing short-circuiting.

In light of the foregoing, there is a need to improve the method of the chemical-mechanical polishing operation.

SUMMARY OF THE INVENTION

Accordingly, the present invention provides a chemical-mechanical polishing process to form a metallic interconnect that is capable of preventing the formation of micro-scratches due to over-polishing or scratching by polishing particles. Consequently, the method is capable of stopping undesirable short-circuiting or cross talks between metallic lines.

To achieve these and other advantages and in accordance with the purpose of the invention, as embodied and broadly described herein, the invention provides a chemical-mechanical polishing (CMP) process. The CMP process includes the steps of providing a semiconductor substrate having a first metallic line thereon, and then forming a first dielectric layer over the substrate and the first metallic line. The first dielectric layer can be a silicon dioxide layer formed using a high-density plasma chemical vapor deposition (HDPCVD) method. Thereafter, a second dielectric layer is formed over the first dielectric layer. The second dielectric layer can be a silicon dioxide layer formed using a plasma-enhanced chemical vapor deposition (PECVD) method. Next, a chemical-mechanical polishing (CMP) operation is carried out to polish the surface of the second dielectric layer. Subsequently, a thin cap layer is formed over the second dielectric layer, in one of several ways, including:

1. A plasma-enhanced chemical vapor deposition (PECVD) method, with silicane (SiH_4) as

the main reactive agent, is used to form a silicon oxide layer having a thickness of about 1000-3000Å, which can be adjusted according to the design rules.

2. A chemical vapor deposition (CVD) method, with tetra-ethyl-ortho-silicate (TEOS) as the main reactive agent, is used to form a silicon dioxide layer having a thickness of about 1000-3000Å, which can be adjusted according to the design rules.

3. A chemical vapor deposition (CVD) method, with silicane (SiH_4) as the main reactive agent, is used to form a silicon nitride layer having a thickness of about 1000-3000Å, which can be adjusted according to the design rules.

4. A chemical vapor deposition (CVD) method, with silicon dichlorohydride (SiH_2Cl_2) as the main reactive agent, is used to form a silicon nitride layer having a thickness of about 1000-3000Å, which can be adjusted according to the design rules.

Thereafter, a via opening is formed through the first dielectric layer, the second dielectric layer and the cap layer, wherein the opening exposes the first metallic line. Finally, a second metallic line is formed over the cap layer and fills the interior of the via opening so that the second metallic line couples electrically with the first metallic line.

It is to be understood that both the foregoing general description and the following detailed description are exemplary, and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention. In the drawings,

Figs. 1A through 1D are cross-sectional views showing the progression of manufacturing

steps in producing a metallic interconnect that uses chemical-mechanical polishing according to a conventional method;

Fig. 2 is a top view showing a conventional metallic interconnect structure; and

Figs. 3A through 3E are cross-sectional views showing the progression of manufacturing steps in producing a metallic interconnect that uses chemical-mechanical polishing according to one preferred embodiment of this invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Reference will now be made in detail to the present preferred embodiments of the invention, examples of which are illustrated in the accompanying drawings. Wherever possible, the same reference numbers are used in the drawings and the description to refer to the same or like parts.

One major aspect of this invention is the coating of a cap layer over the dielectric layer after a chemical-mechanical polishing operation is applied to planarize the dielectric layer. Therefore, a higher degree of surface planarity can be obtained, and micro-scratches on the surface of the dielectric layer due to over-polishing or scratching by polishing particles can be eliminated. Consequently, short-circuiting between metallic lines due the presence of metallic scratch lines is prevented.

In general, high-density plasma chemical vapor deposition (HDPCVD) is a method that combines two basic operations. HDPCVD combines a chemical vapor deposition with an etching operation through physical bombardment by ions. High-density plasma serves to effect the ionization of reactive gases, whose kinetic energy and chemical potential is utilized to break chemical bonds and react with molecules on the surface of the semiconductor substrate. Therefore, a layer of the reactive material is able to deposit over and fill cavities on the semiconductor substrate.

On the other hand, the etching operation in HDPCVD is dependent upon the supply of gaseous argon. Physical bombardment by argon is what causes the formation of a 45° cut at the corners of a trench. Through reactive deposition and physical etching, HDPCVD is capable of controlling the deposition of material into micro-trenches of IMD layer, and hence voids are rarely formed. Therefore, HDPCVD is particularly suitable for use in the process of forming metallic interconnect.

Figs. 3A through 3E are cross-sectional views showing the progression of manufacturing steps in producing a metallic interconnect that uses chemical-mechanical polishing according to one preferred embodiment of this invention. First, as shown in Fig. 3A, a semiconductor substrate 40 is provided. Then, an inter-layer dielectric (ILD) layer 42 is formed over the substrate 40. In the subsequent step, first metallic lines 44, for example, aluminum or polysilicon layers are formed over the ILD layer 42. The first metallic lines 44 can be formed by depositing a metallic layer using, for example, a chemical vapor deposition method or a metal sputtering method.

Thereafter, the metallic layer is patterned to form the first metallic lines. Next, an insulating layer 46 and an inter-metal dielectric (IMD) layer 50 are formed above the ILD layer 42 and the first metallic lines 44. The insulating layer 46 is formed by depositing silicon dioxide over the ILD layer 42 and the first metallic lines 44 using, for example, a high-density plasma chemical vapor deposition (HDPCVD) method.

Due to the presence of the first metallic lines 44 and the characteristic of a HDPCVD deposition, a pyramid-like cross-sectional profile 48 having a height of about 10 KÅ is formed above each first metallic line 44. The IMD layer 50 is formed by depositing silicon dioxide to a thickness of about 20KÅ over the insulating layer 46 using, for example, a plasma-enhanced chemical vapor deposition (PECVD) method.

Next, as shown in Fig. 3B, the surface of the IMD layer 50 is planarized, preferably by polishing using, for example, a chemical-mechanical polishing (CMP) method. Because a CMP

operation can easily lead to over-polishing of the surface of the IMD layer 50 or the scratching of the surface by polishing particles, micro-scratches will appear on the surface of the IMD layer 50. These micro-scratches vary in size and depth, and two such scratches labeled 52a and 52b are shown in Fig. 3B.

Next, as shown in Fig. 3C, a cap layer 54 is formed over the IMD layer 50 so that the micro-scratches 52a and 52b are covered. Hence, insulated scratches 56a and 56b are formed. The cap layer 54 preferably having a thickness of between 1000Å to 3000Å can be made from material including, for example, silicon dioxide, phosphosilicate glass (PSG) or silicon-rich oxide (SRO). Moreover, the thickness of the cap layer 54 can be adjusted according to the design rule. The cap layer represents a major aspect of this invention that can be formed in several ways including: (1) using silicane (SiH_4) as the main reactive agent, a plasma-enhanced chemical vapor deposition (PECVD) method is used to form a silicon oxide layer; or (2) using tetra-ethyl-ortho-silicate (TEOS) as the main reactive agent, a chemical vapor deposition (CVD) method is used to form a silicon dioxide layer; or (3) using silicane (SiH_4) as the main reactive agent, a chemical vapor deposition (CVD) method is used to form a silicon nitride layer; or (4) using silicon dichlorohydride (SiH_2Cl_2) as the main reactive agent, a chemical vapor deposition (CVD) method is used to form a silicon nitride layer.

Next, as shown in Fig. 3D, conventional photolithographic and etching operations are carried out to form an opening 58 through the insulating layer 46, the IMD layer 50 and the cap layer 54. The opening 58 exposes one of the first metallic lines 44 and subsequently will serve as a via.

Next, as shown in Fig. 3E, metallic material, for example, tungsten or other conductive material is deposited over the cap layer and into the opening 58. Thereafter, photolithographic and etching operations are again carried out to pattern the metallic layer, thereby forming second metallic lines 60. Consequently, a metallic interconnect structure is formed.

In summary, the advantages of using the chemical-mechanical polishing process of this invention to fabricate metallic interconnect includes:

1. A higher quality of polished surface is obtained by eliminating micro-scratches on a polished surface due to over-polishing or scratching by polishing particles.

2. The polishing process used in this invention is capable of preventing the formation of metallic scratch lines, thereby eliminating possible short-circuiting pathways between subsequently formed metallic lines.

It will be apparent to those skilled in the art that various modifications and variations can be made to the structure of the present invention without departing from the scope or spirit of the invention. In view of the foregoing, it is intended that the present invention cover modifications and variations of this invention provided they fall within the scope of the following claims and their equivalents.

WHAT IS CLAIMED IS:

1. A chemical-mechanical polishing process, comprising the steps of:

forming a first metal line layer and a dielectric layer over a semiconductor substrate;

polishing the dielectric layer to form a planar surface; and

forming a thin cap layer over the dielectric layer.

2. The process of claim 1, wherein the step of forming the first metal line layer includes depositing doped polysilicon.

3. The process of claim 1, wherein the step of forming the dielectric layer includes a high-density plasma chemical vapor deposition (HDPCVD) method.

4. The process of claim 1, wherein the step of forming the dielectric layer includes a plasma-enhanced chemical vapor deposition (PECVD) method.

5. The process of claim 1, wherein the step of forming the dielectric layer includes depositing silicon dioxide.

6. The process of claim 1, wherein the step of polishing the dielectric layer includes a chemical-mechanical polishing method.

7. The process of claim 1, wherein the step of forming the cap layer includes depositing a silicon oxide layer using a plasma-enhanced chemical vapor deposition (PECVD) method with silicane (SiH_4) as main reactive agent such that the silicon oxide layer has a thickness of about 1000-3000Å, and can be adjusted according to design rules.

8. The process of claim 1, wherein the step of forming the cap layer includes depositing a silicon oxide layer using a chemical vapor deposition (CVD) method with tetra-ethyl-ortho-silicate (TEOS) as main reactive agent such that the silicon oxide layer has a thickness of about 1000-3000Å, and can be adjusted according to design rules.

9. The process of claim 1, wherein the step of forming the cap layer includes depositing a silicon nitride layer using a chemical vapor deposition (CVD) method with silicane (SiH_4) as main

reactive agent such that the silicon nitride layer has a thickness of about 100-3000Å, and can be adjusted according to design rules.

10. The process of claim 1, wherein the step of forming the cap layer includes depositing a silicon nitride layer using a chemical vapor deposition (CVD) method with silicon dichlorohydride (SiH_2Cl_2) as main reactive agent such that the silicon nitride layer has a thickness of about 1000-3000Å, and can be adjusted according to design rules.

11. The process of claim 1, wherein the step of forming the cap layer includes depositing silicon dioxide.

12. The process of claim 1, wherein the step of forming the cap layer includes depositing phosphosilicate glass (PSG).

13. The process of claim 1, wherein the step of forming the cap layer includes depositing silicon-rich oxide (SRO).

14. A method of forming a metallic interconnect, the method comprising the steps of:

providing a semiconductor substrate having a first metallic line thereon;

forming a first dielectric layer over the substrate and the first metallic line;

forming a second dielectric layer over the first dielectric layer;

polishing the surface of the second dielectric layer;

forming a cap layer over the second dielectric layer;

forming a via opening through the first dielectric layer, the second dielectric layer and the cap layer, wherein the opening exposes the first metallic line; and

forming a second metallic line over the cap layer such that the second metallic line couples electrically with the first metallic line through the via.

15. The method of claim 14, wherein the step of forming the first metal line includes depositing doped polysilicon.

16. The method of claim 14, wherein the step of forming the first dielectric layer includes a

high-density plasma chemical vapor deposition (HDPCVD) method.

17. The method of claim 14, wherein the step of forming the second dielectric layer includes a plasma-enhanced chemical vapor deposition (PECVD) method.

18. The method of claim 14, wherein the step of forming the first dielectric layer includes depositing silicon dioxide.

19. The method of claim 14, wherein the step of forming the second dielectric layer includes depositing silicon dioxide.

20. The method of claim 14, wherein the step of polishing the dielectric layer includes a chemical-mechanical polishing method.

21. The method of claim 14, wherein the step of forming the cap layer includes depositing a silicon oxide layer using a plasma-enhanced chemical vapor deposition (PECVD) method with silane (SiH_4) as main reactive agent such that the silicon oxide layer has a thickness of about 1000-3000Å, and can be adjusted according to design rules.

22. The method of claim 14, wherein the step of forming the cap layer includes depositing a silicon oxide layer using a chemical vapor deposition (CVD) method with tetra-ethyl-ortho-silicate (TEOS) as main reactive agent such that the silicon oxide layer has a thickness of about 1000-3000Å, and can be adjusted according to design rules.

23. The method of claim 14, wherein the step of forming the cap layer includes depositing a silicon nitride layer using a chemical vapor deposition (CVD) method with silicane (SiH_4) as main reactive agent such that the silicon nitride layer has a thickness of about 1000-3000Å, and can be adjusted according to design rules.

24. The method of claim 14, wherein the step of forming the cap layer includes depositing a silicon nitride layer using a chemical vapor deposition (CVD) method with silicon dichlorohydride (SiH_2Cl_2) as main reactive agent such that the silicon nitride layer has a thickness of about 1000-3000Å, and can be adjusted according to design rules.

25. The method of claim 14, wherein the step of forming the cap layer includes depositing silicon dioxide.

26. The method of claim 14, wherein the step of forming the cap layer includes depositing phosphosilicate glass (PSG).

27. The process of claim 14, wherein the step of forming the cap layer includes depositing silicon-rich oxide (SRO).

申請日期	
案　　號	
類　　別	

A4
C4

（以上各欄由本局填註）

發明 新型 專利說明書

一、發明 新型 名稱	中　文	化學機械研磨製程
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	代表人 姓　名	曹興誠

裝 訂 線

A5
B5

四、中文發明摘要（發明之名稱：　化學機械研磨製程　）

一種化學機械研磨製程，用於製造金屬內連線，首先提供一半導體基底與其上的第一金屬線層。然後，再形成介電層。接著，進行化學機械研磨法，研磨介電層的表面。之後，在介電層上，形成薄的帽蓋層。帽蓋層的材料可爲二氧化矽、磷矽玻璃或多矽氧化矽層，其厚度在約 1000-3000Å 之間。帽蓋層的形成方法包括：以矽甲烷(SiH_4)爲主或是以原矽酸四乙酯(TEOS)爲主的反應劑，利用化學氣相沈積法，形成氧化矽層；或是以矽甲烷(SiH_4)爲主或是以二氯矽甲烷(SiH_2Cl_2)爲主的反應劑，利用化學氣相沈積法，形成氮化矽層。然後，在介電層與帽蓋層中，形成接觸窗口，與第二金屬線層，其電性連接接觸窗口。

英文發明摘要（發明之名稱：　）

五、發明說明（ 1 ）

本發明是有關於一種金屬內連線(metal interconnects)製程，且特別是有關於一種用於平坦化(planarization)內介電層(Inter Layer Dielectric；ILD)或是內金屬介電層(Inter Metal Dielectric；IMD)的化學機械研磨製程(Chemical Mechanical Polishing；CMP)。

在半導體的製程上，例如超大型積體電路(Very-Large Scale Integration ;VLSI)，或甚至極大型積體電路(Ultra-Large Scale Integration；ULSI)製程，通常會隨著元件的積集度增加，在晶片上製作兩層以上的金屬層，以便於在有限的晶片表面上製作高密度的金屬內連線，以配合日趨精密且複雜的積體電路的發展需求。而金屬內連線結構中，通常都具有內介電層(ILD)或是內金屬介電層(IMD)等，用以作金屬線間的絕緣之用。所以，當元件的設計準則(design rules)越趨細密之後，對這些內介電層(ILD)或是內金屬介電層(IMD)的品質要求，例如對平坦化的要求，也會隨之升高。

一般來說，表面平坦化是處理高密度微影的一項重要技術，因沒有高低落差的平坦表面才能避免曝光散射，而達成精密的圖案轉移(pattern transfer)。平坦化技術主要有旋塗式玻璃法(Spin-On Glass；SOG)與化學機械研磨法(CMP)等二種；但在半導體製程技術進入毫微米(sub-half-micron)之後，旋塗式玻璃法已無法滿足所需求的平坦度，所以化學機械研磨技術是現在唯一能提供超大型積

五、發明說明（2）

體電路(VLSI)，甚至極大型積體電路(ULSI)製程，"全面性平坦化(global planarization)"的一種技術。

請參照第 1A 圖至第 1D 圖，其所繪示的爲習知一種金屬金屬內連線結構製造方法的剖面示意圖。首先，請參照第 1A 圖，提供半導體基底 10，其上形成一內介電層 12(ILD)。接著，在內介電層 12 上形成導電線層 14，例如金屬鋁層或是多晶矽層。並在內介電層 12 與導電線層 14 上沈積絕緣層 16，較佳的是利用高密度電漿化學氣相沉積法(High Density Plasma-CVD；HDP-CVD)來形成，因此容易在導電線層 14 的上方形成金字塔形剖面 18 的結構。然後，在絕緣層 16 上覆蓋內金屬介電層 19(IMD)。

接著，請參照第 1B 圖，進行化學機械研磨法(CMP)，研磨內金屬介電層 19 的表面，用以平坦化內金屬介電層 19 的表面。此時，由於化學機械研磨法容易產生過拋的情形(overpolishing)，或是由於研磨粒子損傷晶片的表面，而導致微刮(micro-scratch)的現象。因此，會在內金屬介電層 19 的表面形成一些深度與尺寸大小不一的刮痕，例如刮痕 20a 與 20b。

接著，請參照第 1C 圖，繼續後面的製程，包括進行微影與蝕刻等定義圖案的步驟，在絕緣層 16 與內金屬介電層 19 中蝕刻出開口 22，露出導電線層 14。開口 22 用以作介層窗口(via)之用。

接著，請參照第 1D 圖，在開口 22 中與內金屬介電層 19 上形成金屬層 26。並進行微影與蝕刻步驟，定義此金

五、發明說明(3.)

屬層 26 的圖案，形成第二層的金屬線層 26。由於在內金屬介電層 19 的表面有刮痕 20a 與 20b 等存在，因此亦會在刮痕 20a 與 20b 中填入金屬層，而形成金屬刮痕 24a 與 24b。

上述餘留的金屬刮痕容易造成一些缺點，如第 2 圖所示，其所繪示的爲習知一種金屬內連線結構的俯視示意圖。其中，在半導體基底(未顯示)上，設有第一導電線層 30，例如金屬鋁層或是多晶矽層。在第一導電線層 30 上，還設有第二導電線層 32，而第一導電線層 30 透過介層窗 33 與第二導電線層 32 電性連接。若是在起初研磨第一導電線層 30 表面時，產生過拋的情形，形成了金屬刮痕 34。於是容易因此金屬刮痕 34 的存在，而導致後續金屬線(例如第二導電線層 32)的導通短路情形。

有鑑於此，本發明的主要目的就是在提供一種化學機械研磨製程，用於製作金屬內連線，其可以防止由於過拋情形或研磨粒子損傷晶片的表面，所導致的微刮現象，消除金屬線間不當的短路或交流情形(cross-talk)。

爲達成上述之目的，本發明提出一種化學機械研磨製程，首先提供一半導體基底，在其上已形成第一金屬線層。然後，在半導體基底與第一金屬線層上，形成第一介電層，第一介電層的材料可爲二氧化矽，其形成方法例如高密度電漿化學氣相沈積法(HDP-CVD)。再於該第一介電層上，形成第二介電層，第二介電層的材料可爲二氧化矽，其形成方法爲電漿加強式化學氣相沈積法(PECVD)。

五、發明說明（4）

接著，進行化學機械研磨法(CMP)，研磨第二介電層的表面。之後，在第二介電層上，形成薄的帽蓋層。帽蓋層的形成方法包括：(1)以矽甲烷(SiH_4)爲主的反應劑，利用電漿加強式化學氣相沈積法(PECVD)，形成氧化矽層，厚度在約 1000-3000Å 之間，可依設計準則的厚度需要而作調整；或是(2)以原矽酸四乙酯(TEOS)爲主的反應劑，利用化學氣相沈積法(CVD)，形成氧化矽層，厚度在約 1000-3000Å 之間，可依設計準則的厚度需要而作調整；或是(3)以矽甲烷(SiH_4)爲主的反應劑，利用化學氣相沈積法(CVD)，形成氮化矽層，厚度在約 1000-3000Å 之間，可依設計準則的厚度需要而作調整；或是(4)以二氯矽甲烷(SiH_2Cl_2)爲主的反應劑，利用化學氣相沈積法(CVD)，形成氮化矽層，厚度在約 1000-3000Å 之間，可依設計準則的厚度需要而作調整。然後，在第一介電層、第二介電層與帽蓋層中，形成接觸窗口，露出第一金屬線層。以及在帽蓋層上與接觸窗口中，形成第二金屬線層，其電性連接接觸窗口。

爲讓本發明之上述和其他目的、特徵、和優點能更明顯易懂，下文特舉一較佳實施例，並配合所附圖式，作詳細說明如下：

圖式之簡單說明：

第 1A 圖至第 1D 圖，其所繪示的爲習知一種金屬內連線製造流程的剖面示意圖；

第 2 圖，其所繪示的爲習知一種金屬內連線結構的俯

五、發明說明（ 5 ）

視示意圖；以及

第 3A 圖至第 3E 圖，其所繪示的爲根據本發明之一較佳實施例，一種金屬內連線製造流程的剖面示意圖。

其中，各圖示之標號所代表的元件結構如下：

10,40：半導體基底

12,42：內介電層(ILD)

14,30：第一層導電線層

16,46：絕緣層

18,48：金字塔形剖面

19,50：內金屬介電層(IMD)

20a,20b,52a,52b：刮痕

22,33：接觸窗口

24a,24b,34：金屬刮痕

26,32：第二層導電線層

實施例

本發明的特徵是，在進行化學機械研磨步驟之後，再鋪蓋一層帽蓋層(cap layer)於介電層上，使得平坦化步驟的品質更佳，可避免由於化學機械研磨法產生過拋的情形(overpolishing)，或是由於研磨粒子損傷晶片的表面，而導致微刮(micro-scratch)的現象。消除介電層上的刮痕與後續金屬線的導通短路情形。

一般來說，高密度電漿化學氣相沉積法(HDP-CVD)的原理描述如下：此法爲兩種製程的結合，即化學沉積和物理轟擊蝕刻兩種製程同時發生。沉積的製程主要藉由誘發

五、發明說明（6）

高電子密度電漿促進反應氣體的離化效率(ionization efficiency)，再利用反應離子的動能和化學能，打破半導體基底表面的鍵結，進行反應而沉積於半導體基底上，產生溝填的作用。至於蝕刻的製程，主要決定於氬氣，其物理轟擊蝕刻是造成溝渠轉角 45^0 切面的主因。由於沉積反應與物理蝕刻的搭配，高密度電漿化學氣相沉積法可以控制於微小的金屬間隙介電層溝填應用，而不易造成孔洞，非常適用於目前的金屬內連線製程。

請參照第 3A 圖至第 3E 圖，其所繪示的爲根據本發明之一較佳實施例，一種金屬內連線製造流程的剖面示意圖。首先，請參照第 3A 圖，提供半導體基底 40，在半導體基底 40 上形成內介電層 42(ILD)。然後，在第一介電層 42 上，形成第一金屬線層 44，其材料可爲金屬鋁或摻雜的多晶矽，且形成方式例如爲化學氣相沈積法或金屬濺鍍法，然後再定義此第一金屬線層 44 的圖案。接著，在內介電層 42 與第一金屬線層 44 上，形成絕緣層 46 與內金屬介電層 50(IMD)。其中，絕緣層 46 的材料例如爲二氧化矽，其形成方法例如爲高密度電漿化學氣相沈積法(HDP-CVD)。由於高密度電漿化學氣相沉積法的特性，在每個第一金屬線層 44 上方會形成凸出的結構，其高度例如爲約 10KÅ 左右，例如尖銳的金字塔形剖面結構 48，如第 3A 圖所示。而內金屬介電層 50 的材料例如爲二氧化矽，其厚度例如爲約 20KÅ 左右，且其形成方法例如爲電漿加強式化學氣相沈積法(PECVD)。

五、發明說明（ 7 ）

接著，請參照第 3B 圖，進行平坦化的步驟，平坦化內金屬介電層 50 的表面。其方式較佳的是進行研磨步驟，例如爲化學機械研磨法(CMP)，磨平內金屬介電層 50 的表面。由於化學機械研磨法容易產生過拋的情形，或是由於研磨粒子損傷晶片的表面，而導致微刮的現象。因此，會在內金屬介電層 50 的表面形成一些深度與尺寸大小不一的刮痕，例如刮痕 52a 與 52b。

接著，請參照第 3C 圖，在內金屬介電層 50 上形成帽蓋層 54，用以覆蓋住刮痕 52a 與 52b，使得在刮痕處都填滿帽蓋層 54，形成絕緣刮痕 56a 與 56b。帽蓋層 54 的材料例如爲二氧化矽、磷矽玻璃(Phosphate Silicon Glass；PSG)或多矽氧化矽層(Silicon Riched Oxide；SRO)，其厚度較佳的是在約 1000-3000Å 之間，可依設計準則的厚度需要而作調整。此帽蓋層 54 爲本發明的特徵，其形成方法有許多種，一一列舉描述如下：(1)帽蓋層 54 的形成方法可爲以矽甲烷(SiH_4)爲主的反應劑，利用化學氣相沈積法(CVD)，而形成氧化矽層；(2)或是帽蓋層 54 的形成方法可爲以原矽酸四乙酯(TEOS)爲主的反應劑，利用電漿加強式化學氣相沈積法(PECVD)，而形成二氧化矽層；(3)帽蓋層 54 的形成方法可爲以矽甲烷(SiH_4)爲主的反應劑，利用化學氣相沈積法(CVD)，而形成氮化矽層；(4)或是帽蓋層 54 的形成方法可爲以二氯矽甲烷(SiH_2Cl_2)爲主的反應劑，利用化學氣相沈積法(CVD)，而形成氮化矽層。

五、發明說明(8)

接著，請參照第 3D 圖，進行微影與蝕刻步驟，在絕緣層 46、內金屬介電層 50 與帽蓋層 54 中形成開口 58，暴露出第一金屬線層 44。此開口 58 對應預定形成金屬介層窗(via)的位置，

接著，請參照第 3E 圖，在開口 58 中填入導電材料，例如金屬鎢或其他導電材料，可用以電性連接上下兩層金屬層。以及在帽蓋層 54 上與接觸窗口 58 中，形成第二金屬線層 60，於是完成本發明之金屬內連線結構。

綜上所述，本發明所提出之化學機械研磨製程，用於製造金屬內連線，具有以下的好處：

(1)本發明所提出之化學機械研磨製程，可使得平坦化的品質更佳，避免由於化學機械研磨法產生過拋的情形，或是由於研磨粒子損傷晶片的表面，而導致微刮的現象。

(2)本發明所提出之化學機械研磨製程，可消除介電層上之後續金屬線因刮痕而導致的短路情形。

綜上所述，雖然本發明已以一較佳實施例揭露如上，然其並非用以限定本發明，任何熟習此技藝者，在不脫離本發明之精神和範圍內，當可作各種之更動與潤飾，因此本發明之保護範圍當視後附之申請專利範圍所界定者爲準。

六、申請專利範圍.

1.一種化學機械研磨製程，其中在一半導體基底上，依序形成有一第一金屬線層與一介電層，該製程包括下列步驟：

進行一研磨步驟，將該介電層的表面磨平；以及

形成一薄的帽蓋層，在該介電層的表面上。

2.如申請專利範圍第 1 項所述之製程，其中該第一金屬線層包括摻雜的多晶矽。

3.如申請專利範圍第 1 項所述之製程，其中該介電層的形成方法包括高密度電漿化學氣相沈積法(HDP-CVD)。

4.如申請專利範圍第 1 項所述之製程，其中該介電層的形成方法包括電漿加強式化學氣相沈積法(PECVD)。

5.如申請專利範圍第 1 項所述之製程，其中該介電層包括二氧化矽。

6.如申請專利範圍第 1 項所述之製程，其中該研磨步驟包括化學機械研磨法。

7.如申請專利範圍第 1 項所述之製程，其中該帽蓋層的形成方法包括以矽甲烷(SiH_4)爲主的反應劑，利用電漿加強式化學氣相沈積法(PECVD)，形成氧化矽層，厚度在約 1000-3000Å 之間，可依設計準則的厚度需要而作調整。

8.如申請專利範圍第 1 項所述之製程，其中該帽蓋層的形成方法包括以原矽酸四乙酯(TEOS)爲主的反應劑，利用化學氣相沈積法(CVD)，形成氧化矽層，厚度在約 1000-3000Å 之間，可依設計準則的厚度需要而作調整。

9.如申請專利範圍第 1 項所述之製程，其中該帽蓋層

六、申請專利範圍.

的形成方法包括以矽甲烷(SiH_4)爲主的反應劑，利用化學氣相沈積法(CVD)，形成氮化矽層，厚度在約 1000-3000Å 之間，可依設計準則的厚度需要而作調整。

10.如申請專利範圍第 1 項所述之製程，其中該帽蓋層的形成方法包括以二氯矽甲烷(SiH_2Cl_2)爲主的反應劑，利用化學氣相沈積法(CVD)，形成氮化矽層，厚度在約 1000-3000Å 之間，可依設計準則的厚度需要而作調整。

11.如申請專利範圍第 1 項所述之製程，其中該帽蓋層的材料包括二氧化矽。

12.如申請專利範圍第 1 項所述之製程，其中該帽蓋層的材料包括磷矽玻璃(PSG)。

13.如申請專利範圍第 1 項所述之製程，其中該帽蓋層的材料包括多矽氧化矽層(SRO)。

14.一種金屬內連線製程，該製程包括下列步驟：

提供一半導體基底，在該半導體基底上已形成一第一金屬線層；

形成一第一介電層，在該半導體基底與該第一金屬線層上；

形成一第二介電層，在該第一介電層上；

進行一研磨步驟，研磨該第二介電層的表面；

形成一帽蓋層，在該第二介電層上；

形成一接觸窗口，在該第一介電層、該第二介電層與該帽蓋層中，露出該第一金屬線層；以及

形成一第二金屬線層，在該帽蓋層上，並電性連接該

六、申請專利範圍.

接觸窗口。

15.如申請專利範圍第 14 項所述之製程，其中該第一金屬線層包括摻雜的多晶矽。

16.如申請專利範圍第 14 項所述之製程，其中該第一介電層的形成方法包括高密度電漿化學氣相沈積法(HDP-CVD)。

17.如申請專利範圍第 14 項所述之製程，其中該第二介電層的形成方法包括電漿加強式化學氣相沈積法(PECVD)。

18.如申請專利範圍第 14 項所述之製程，其中該第一介電層包括二氧化矽。

19.如申請專利範圍第 14 項所述之製程，其中該第二介電層包括二氧化矽。

20.如申請專利範圍第 14 項所述之製程，其中該研磨步驟包括化學機械研磨法。

21.如申請專利範圍第 14 項所述之製程，其中該帽蓋層的形成方法包括以矽甲烷(SiH_4)爲主的反應劑，利用電漿加強式化學氣相沈積法(PECVD)，形成氧化矽層，厚度在約 1000-3000Å 之間，可依設計準則的厚度需要而作調整。

22.如申請專利範圍第 14 項所述之製程，其中該帽蓋層的形成方法包括以原矽酸四乙酯(TEOS)爲主的反應劑，利用化學氣相沈積法(CVD)，形成氧化矽層，厚度在約 1000-3000Å 之間，可依設計準則的厚度需要而作調整。

六、申請專利範圍.

23.如申請專利範圍第 14 項所述之製程，其中該帽蓋層的形成方法包括以矽甲烷(SiH_4)爲主的反應劑，利用化學氣相沈積法(CVD)，形成氮化矽層，厚度在約 1000-3000Å 之間，可依設計準則的厚度需要而作調整。

24.如申請專利範圍第 14 項所述之製程，其中該帽蓋層的形成方法包括以二氯矽甲烷(SiH_2Cl_2)爲主的反應劑，利用化學氣相沈積法(CVD)，形成氮化矽層，厚度在約 1000-3000Å 之間，可依設計準則的厚度需要而作調整。

25.如申請專利範圍第 14 項所述之製程，其中該帽蓋層的材料包括二氧化矽。

26.如申請專利範圍第 14 項所述之製程，其中該帽蓋層的材料包括磷矽玻璃(PSG)。

27.如申請專利範圍第 14 項所述之製程，其中該帽蓋層的材料包括多矽氧化矽層(SRO)。